

**Engineering and Technology Industry Council**  
**New Initiative Proposal**  
**Biennium from July 1, 2005 to June 30, 2007**

**Campus:** Portland State University  
**Contact Name:** Robert D. Dryden, Dean  
**Date of Submission:** April 2, 2004  
**Summary of Proposal:** Create Associate Dean for Research –  
Launch Research Initiative with Industry Partners

**Goals/Investment Description/Results**

The College of Engineering and Computer Science at Portland State University is positioned to make a significant step forward in sponsored research. Our new faculty are excellent and all our research activity.

Without additional support and resources, however, our projected rate of research growth, although impressive, will be less than our potential. Infrastructure support, in the right area, will accelerate our rate of growth.

We are proposing the establishment of an Associate Dean for Research in CECS. This individual will mentor junior faculty and support external funding contacts and discussions necessary to take junior faculty from modest, annual funding to significant, multi-year awards.

This individual will be a senior faculty member with tenure in a CECS department. This individual will also have unique expertise in areas of growth that are critical to the College and the University. In our case, the ideal candidate will be able to move our instruction and academic agenda forward for key firms such as Intel, LSI Logic, and other semiconductor companies. This individual will, of course, require start-up funds and some initial graduate student support.

The following paragraphs outline a course of action to forge a new relationship between PSU and the semiconductor industry. This type of relationship will strengthen the University and provide services directly to key clients.

Moore's law has been with us for many years and has led to an incredible revolution in integrated circuit complexity and computer technology. However, going forward we are starting to approach the limits of traditional CMOS technology. To continue scaling we will need to move to molecular scale computing with devices that operate at the nanometer scales. This transition will have a tremendous impact on all aspects of computer engineering and computing science itself. For example, nano-scale devices will offer more parallelism than speed, as well as significant connectivity limitations. In addition, they will have a level of hardware faults than we have with existing CMOS technology.

Though many proposed nanotechnologies are of a revolutionary nature, it is most likely that early nano-scale implementation will be hybrid with existing silicon technology, expanding incrementally over a period of time. For example, we may start with simple embedded nano-grids used as very dense memory and

programmable logic. Such a path would also allow a more incremental approach to the newer more highly parallel algorithms/applications. By embedding in existing CMOS, we can use CMOS to compensate for some of the things that molecular scale devices do not do well, such as inversion and amplification, and the use of CMOS for long range connections between the nano-scale subunits, etc.

Depending on how nano-grids are used, the fault tolerance issue could still be a problem. The density advantage of molecular scale computing is going to be at risk if significant redundancy is required to make the technology useful for existing applications. An effective way to gain fault tolerance without significant hardware redundancy is if the algorithms and applications themselves are fault tolerant. Many adaptive signal processing and control algorithms are insensitive to a variety of computational faults. And, if we believe that interfacing computers to the real world (e.g., computer vision or speech recognition) constitute major application areas, these are very likely the kinds of algorithms that could constitute the majority of computation in 10-20 years, making molecular scale even more attractive.

In addition to incredible computational density, working at the nanoscale raises a number of potential problems, not the least of which is manufacturing and test. A working program in nanoscale design will require experts from a number of different areas in PSU. This will allow close collaboration with groups in Physics and Chemistry who are working with nano-scale devices. Nanoscale technology is important to key industrial partners, such as Intel and LSI Logic.

## **Proposed Investment and Private Support Forecast (\$M)**

	7/1/05- 6/30/06	7/1/06- 6/30/07	Total
<b>Proposed OUS Investment (\$M)</b>			
Associate Dean for Research	0.23	0.23	0.46
Travel & Other Support	0.05	0.05	0.10
Graduate Student Support (3)	0.06	0.06	0.12
Associate Dean Set-up	0.25	0.25	0.50
Junior Faculty Addition	0.15	0.15	0.30
Junior Faculty Start-up	0.05	0.05	0.10
Subtotal	0.79	0.79	1.58
Expected private support (\$M) (2)	1.19	1.19	2.37
<b>Total (\$M)</b>	1.98	1.98	3.96
<b>New Faculty Supported (FTE) (3)</b>	2.0	2.0	2.0

**Metrics Forecast:**

	Baseline	Projected			
	AY 99	AY06	AY07	AY08	AY09
Total Research Volume	\$1.8M	\$5.0M	\$5.95M	\$6.9M	\$7.64M
ECS Graduate Student Credit Hourse	8685	19807	20460	21960	23407

**Notes:**  
(1) List metrics including those relevent from Core Proposal template and others relevent to your proposal. If you use a metric that is also covered in your Core Proposal, the forecasted results that you give above should be the combined result of your Core Proposal and the investment described in this document.